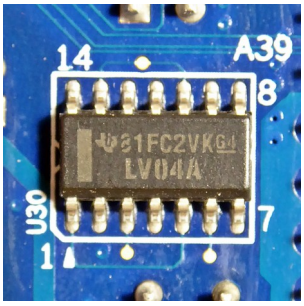
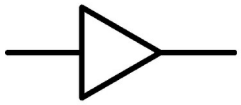
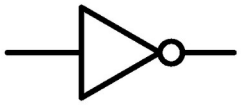
Logic gate symbols and truth tables





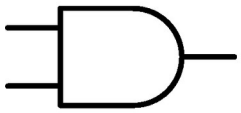
X	Y
0	0
1	1

Buffer



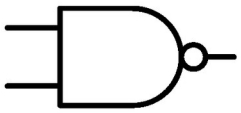
X	Y
0	1
1	0

Inverter or NOT gate



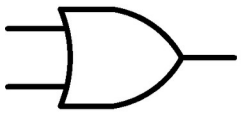
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

AND gate



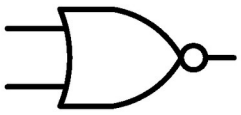
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NAND gate



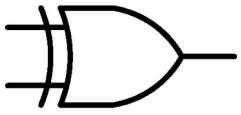
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

OR gate



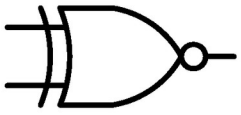
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

NOR gate



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Exclusive-OR gate



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Exclusive-NOR gate