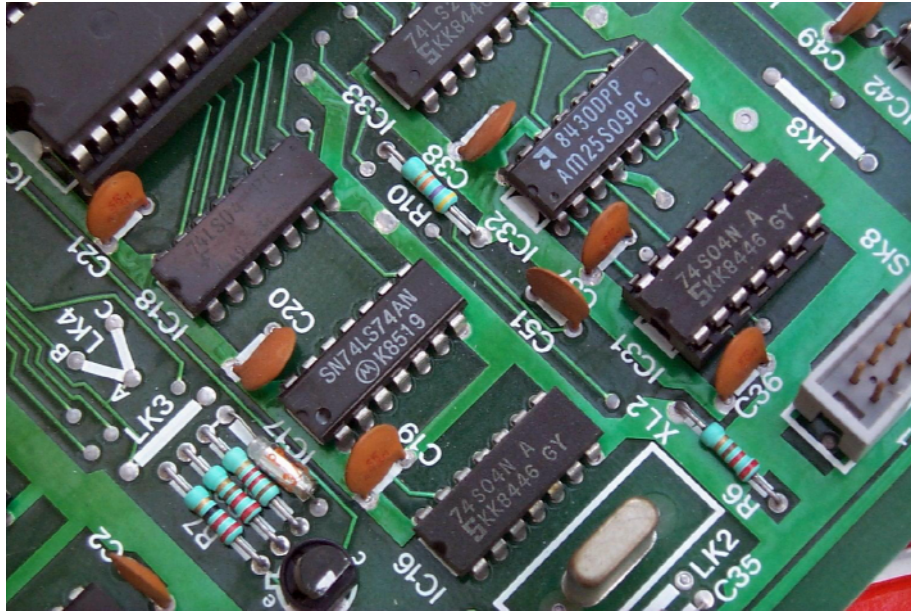


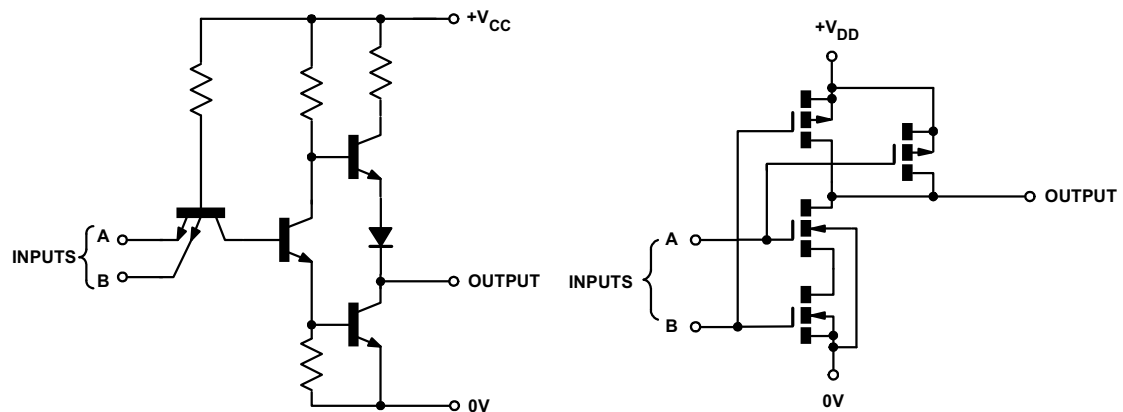
## Logic families

Digital integrated circuit devices are often classified according to the semiconductor technology used in their manufacture; the logic family to which a device belongs being largely instrumental in determining its operational characteristics (such as power consumption, speed, and immunity to noise).



Logic gates are often supplied in 14-pin dual-in-line packages

The two basic logic families are CMOS (Complementary Metal Oxide Semiconductor) and TTL (Transistor Transistor Logic). Each of these families is then further sub-divided. Representative circuits of a two-input AND gate in both technologies is shown in the figure below. The most common family of TTL logic devices is known as the 74-series. Devices from this family are coded with the prefix number 74.



(a) TTL two-input AND gate

(b) CMOS two-input AND gate

Variants within the family are identified by letters that follow the initial 74 prefix, as follows:

<i>Infix</i>	<i>Meaning</i>
none	Standard TTL device.
ALS	Advanced low-power Schottky*
C	CMOS version of a TTL device
F	'Fast' - a high speed version of the device.
H	High speed version.
S	Schottky input configuration (improved speed and noise immunity).
HC	High speed CMOS version (CMOS compatible inputs).
HCT	High speed CMOS version (TTL compatible inputs)
LS	Low-power Schottky*

\* Schottky diodes/transistors have better switching characteristics than conventional devices

The most common family of CMOS devices is known as the 4000-series. Variants within the family are identified by suffix letters as follows:

<i>Suffix</i>	<i>Meaning</i>
none	Standard CMOS device
A	Standard (unbuffered) CMOS device
B, BE	Improved (buffered) CMOS device
UB, UBE	Improved (unbuffered) CMOS device.

### *Example*

Identify each of the following integrated circuits:

- (i) 4001UBE
- (ii) 74LS14

### *Solution*

Integrated circuit (i) is an improved (unbuffered) version of the CMOS 4001 device. Integrated circuit (ii) is a low-power Schottky version of the TTL 7414 device.

### *Question*

How many devices can you identify in the photograph on the first page?

## Logic circuit characteristics

Logic levels are simply the range of voltages used to represent the logic states 0 and 1. The logic levels for CMOS differ markedly from those associated with TTL. In particular, CMOS logic levels are relative to the supply voltage used whilst the logic levels associated with TTL devices tend to be absolute. The following table usually applies:

	CMOS	TTL
Logic 1	more than $\frac{2}{3}V_{DD}$	more than 2V
Logic 0	less than $\frac{1}{3}V_{DD}$	less than 0.8V
Indeterminate	between $\frac{1}{3}V_{DD}$ and $\frac{2}{3}V_{DD}$	between 0.8V and 2V

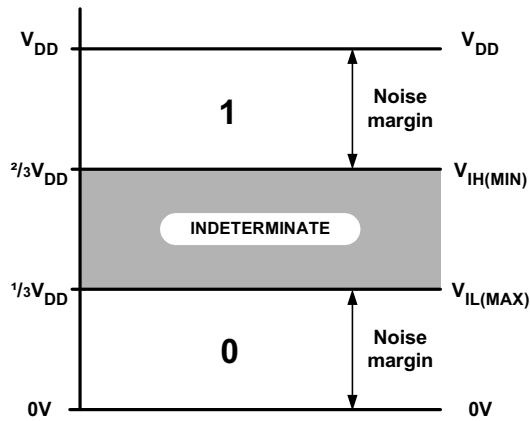
Note:  $V_{DD}$  is the positive supply associated with CMOS devices

The *noise margin* is an important feature of any logic device. Noise margin is a measure of the ability of the device to reject noise; the larger the noise margin the better is its ability to perform in an environment in which noise is present. Noise margin is defined as the difference between the minimum values of high state output and high state input voltage and the maximum values of low state output and low state input voltage. Hence:

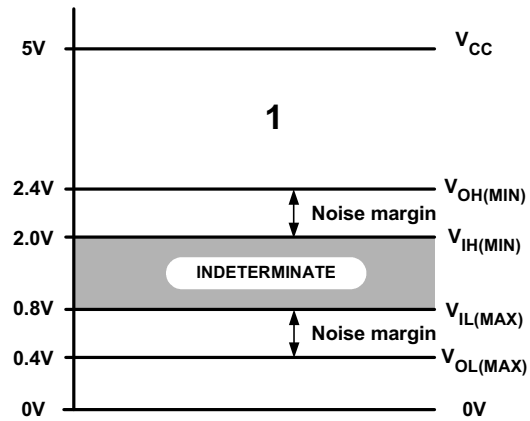
$$\text{Noise margin} = V_{OH(MIN)} - V_{IH(MIN)}$$

$$\text{or noise margin} = V_{OL(MAX)} - V_{IL(MAX)}$$

Where  $V_{OH(MIN)}$  is the minimum value of high state (logic 1) output voltage,  $V_{IH(MIN)}$  is the minimum value of high state (logic 1) input voltage,  $V_{OL(MAX)}$  is the maximum value of low state (logic 0) output voltage, and  $V_{IL(MIN)}$  is the minimum value of low state (logic 0) input voltage. The noise margin for standard 7400 series TTL is typically 400 mV whilst that for CMOS is  $\frac{1}{3}V_{DD}$ , as shown on the next page.



**CMOS**



**TTL**

The following table compares the more important characteristics of various members of the TTL family with buffered CMOS logic:

<i>Characteristic</i>	<i>Logic family</i>			
	74	74LS	74HC	40BE
Maximum supply voltage	5.25V	5.25V	5.5V	18V
Minimum supply voltage	4.75V	4.75V	4.5V	3V
Static power dissipation (mW per gate at 100kHz)	10	2	negligible	negligible
Dynamic power dissipation (mW per gate at 100kHz)	10	2	0.2	0.1
Typical propagation delay (ns)	10	10	10	105
Maximum clock frequency (MHz)	35	40	40	12
Speed-power product (pJ at 100kHz)	100	20	1.2	11
Minimum output current (mA at $V_{OUT} = 0.4V$ )	16	8	4	1.6
Fan-out (LS loads)	40	20	10	4
Maximum input current (mA at $V_{IN} = 0.4V$ )	-1.6	-0.4	0.001	-0.001

Note: The forerunners of TTL technology were DL (diode logic) and RTL (resistor transistor logic). Both of these technologies are now well and truly obsolete!

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September 2003